EV2A16A
256K x 16-bit 3.3V Asynchronous Magnetoresistive RAM

Datasheet

Features

- **Single 3.3V Power Supply**
- **Industrial Temperature Range (–40°C to 110°C) and Military Temperature Range (–55°C to 125°C)**
- **Symmetrical High-speed Read and Write with Fast Access Time (35 ns)**
- **Flexible Data Bus Control: 8 bit or 16 bit Access**
- **Equal Address and Chip-enable Access Times**
- **Automatic Data Protection with Low-voltage Inhibit Circuitry to Prevent Writes on Power Loss**
- **All Inputs and Outputs are Transistor-transistor Logic (TTL) Compatible**
- **Fully Static Operation**
- **Full Nonvolatile Operation with 20 Years Minimum Data Retention**

Introduction

The EV2A16A is a 4,194,304-bit magnetoresistive random access memory (MRAM) device organized as 262,144 words of 16 bits. The EV2A16A is equipped with chip enable ($\overline{E}$), write enable ($\overline{W}$), and output enable ($\overline{G}$) pins, allowing for significant system design flexibility without bus contention. Because the EV2A16A has separate byte-enable controls ($\overline{LB}$ and $\overline{UB}$), individual bytes can be written and read.

MRAM is a nonvolatile memory technology that protects data in the event of power loss and does not require periodic refreshing. The EV2A16A is the ideal memory solution for applications that must permanently store and retrieve critical data quickly.

The EV2A16A is available in a 400-mil, 44-lead plastic small-outline TSOP type-II package RoHS compliant (MSL3 according to Jedec standard) with an industry-standard center power and ground SRAM pinout.

The EV2A16A is available in Industrial (–40°C to 110°C) and Military (–55°C to +125°C) temperature ranges.

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for the latest version of the datasheet

1. Device Pin Assignment

Figure 1-1. Block Diagram

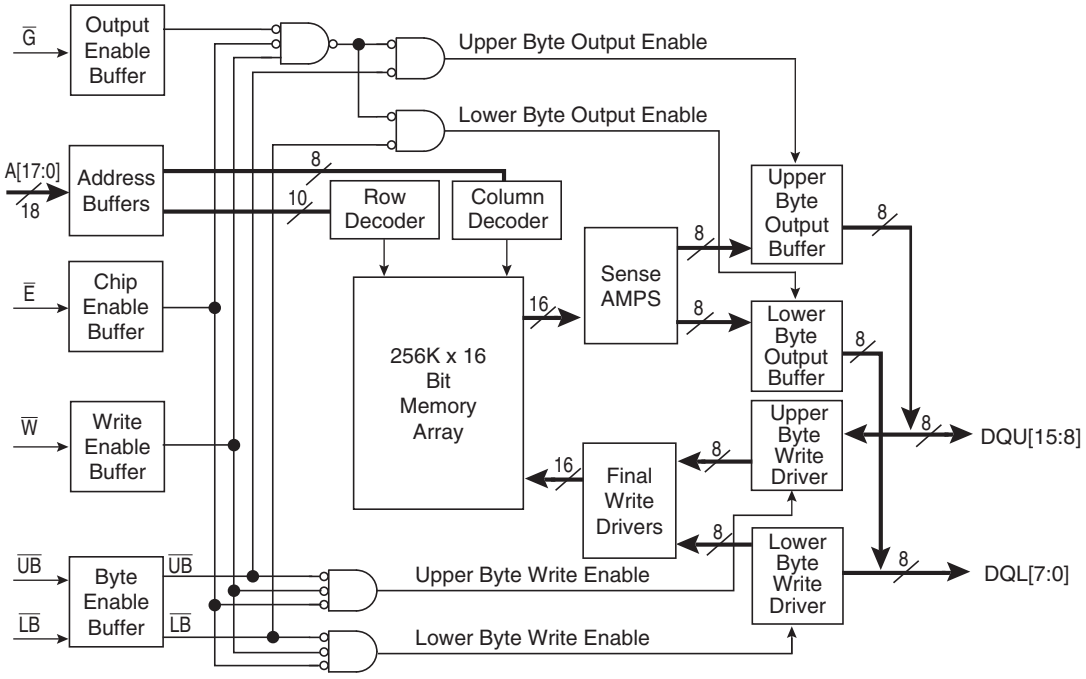
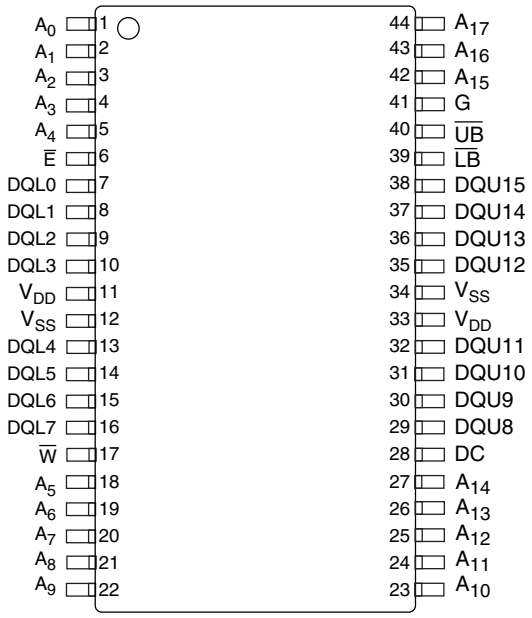


Table 1-1. Pin Functions

Signal Name	Function
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{UB}$	Upper Byte Enable
$\overline{LB}$	Lower Byte Enable
DQ	Data I/O
V_{DD}	Power Supply
V_{SS}	Ground
DC	Do Not Connect
NC	No Connection

Figure 1-2. Pin Diagrams for Available Packages (Top View)



44-Pin TSOP Type2

Table 1-2. Operating Modes

$\overline{E}$[1]	$\overline{G}$[1]	$\overline{W}$[1]	$\overline{LB}$[1]	$\overline{UB}$[1]	Mode	V_{DD} Current	DQL[7:0][2]	DQU[15:8][2]
H	X	X	X	X	Not selected	I_{SB1}, I_{SB2}	Hi-Z	Hi-Z
L	H	H	X	X	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	X	X	H	H	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	L	H	L	H	Lower Byte Read	I_{DDR}	D_{Out}	Hi-Z
L	L	H	H	L	Upper Byte Read	I_{DDR}	Hi-Z	D_{Out}
L	L	H	L	L	Word Read	I_{DDR}	D_{Out}	D_{Out}
L	X	L	L	H	Lower Byte Write	I_{DDW}	D_{in}	Hi-Z
L	X	L	H	L	Upper Byte Write	I_{DDW}	Hi-Z	D_{in}
L	X	L	L	L	Word Write	I_{DDW}	D_{in}	D_{in}

Notes: 1. H = high, L = low, X = don't care
2. Hi-Z = high impedance

2. Electrical Specifications

2.1 Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 2-1. Absolute Maximum Ratings(1)

Symbol	Parameter	Temp Range	Package	Value	Unit
V_{DD}	Supply voltage (2)	–	–	–0.5 to 4.0	V
V_{IN}	Voltage on any pin (2)	–	–	–0.5 to V_{DD} + 0.5	V
I_{OUT}	Output current per pin	–	–	±20	mA
P_D	Package power dissipation (3)	–	Note (3)	0.600	W
T_{BIAS}	Temperature under bias	Industrial	–	–40 to 110	°C
		Military	–	–55 to 125	
T_{stg}	Storage Temperature	–	–	–55 to 150	°C
T_{Lead}	Lead temperature during solder (3 minute max)	–	–	260	°C
H_{max_write}	Maximum magnetic field during write	Industrial, Military	TSOP2	2000	A/m
H_{max_read}	Maximum magnetic field during read or standby	Industrial, Military	TSOP2	8000	A/m

Notes:
1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
2. All voltages are referenced to V_{SS}.
3. Power dissipation capability depends on package characteristics and use environment.

Table 2-2. Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Power supply voltage(1)	V_{DD}	3.0(1)	3.3	3.6	V
Write inhibit voltage	V_{WI}	2.5	2.7	3.0(1)	V
Input high voltage	V_{IH}	2.2	–	V_{DD} + 0.3(2)	V
Input low voltage	V_{IL}	–0.5(3)	–	0.8	V
Operating temperature	Tcase	–40 –55		+110 +125	°C

Notes:
1. There is a 2 ms startup time once V_{DD} exceeds V_{DD},(max). See **Power Up and Power Down Sequencing** below.
2. V_{IH}(max) = V_{DD} + 0.3 V_{DC} ; V_{IH}(max) = V_{DD} + 2.0 V_{AC} (pulse width ≤ 10 ns) for I ≤ 20.0 mA.
3. V_{IL}(min) = –0.5 V_{DC} ; V_{IL}(min) = –2.0 V_{AC} (pulse width ≤ 10 ns) for I ≤ 20.0 mA.

2.2 Power-up and Power-down Sequencing

The MRAM is protected from write operations whenever V_{DD} is less than V_{WI}. As soon as V_{DD} exceeds V_{DD}(min), there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The $\overline{E}$ and $\overline{W}$ control signals should track V_{DD} on power up to V_{DD} – 0.2 V or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that signal remains high if the driving signal is Hi-Z during power up. Any logic that drives E and W should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where V_{DD} goes below V_{WI}, writes are protected and a startup time must be observed when power returns above V_{DD}(min).

Figure 2-1. Power Up and Power Down Diagram

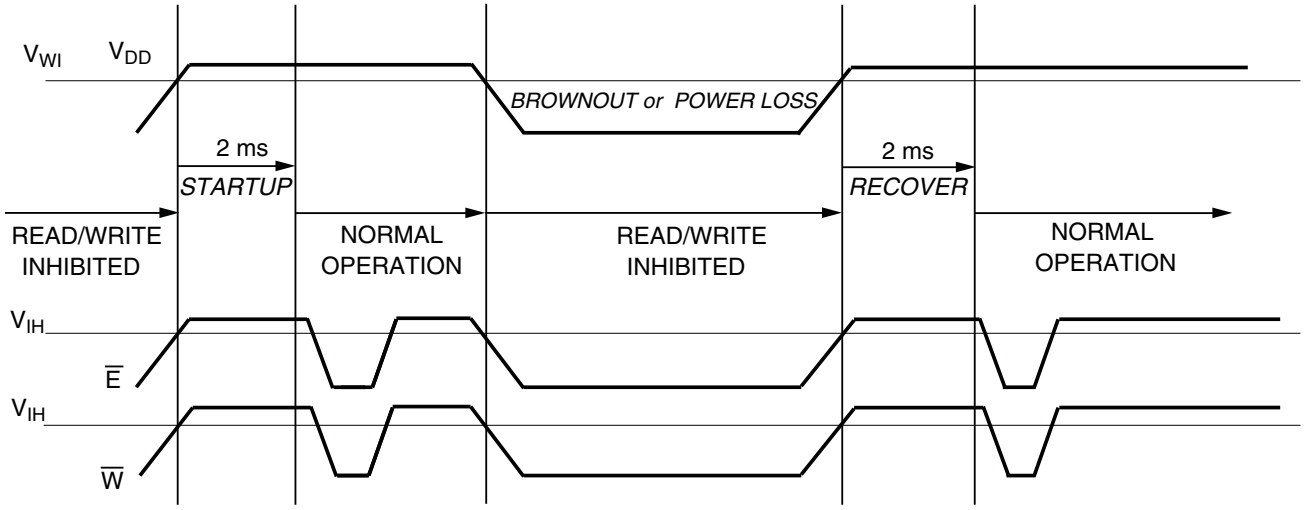


Table 2-3. DC Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Input leakage current	$I_{lkg(I)}$	–	–	±1	µA
Output leakage current	$I_{lkg(O)}$	–	–	±1	µA
Output low voltage (I_{OL} = +4 mA) (I_{OL} = +100 µA)	V_{OL}	–	–	0.4 V_{SS} + 0.2	V
Output high voltage (I_{OH} = –4 mA) (I_{OH} = –100 µA)	V_{OH}	2.4 V_{DD} – 0.2	–	–	V

Table 2-4. Power Supply Characteristics

Parameter	Symbol	Typical	Max	Unit
AC active supply current – read modes[1] (I_{OUT} = 0 mA, V_{DD} = max)	I_{DDR}	55	80	mA
AC active supply current – write modes[1] (V_{DD} = max) Industrial Grade Military Grade	I_{DDW}	 105 105	 165 165	mA
AC standby current (V_{DD} = max, $\overline{E}$ = V_{IH}) *no other restrictions on other inputs*	I_{SB1}	18	28	mA
CMOS standby current ($\overline{E} \geq V_{DD} - 0.2V$ and $V_{In} \leq V_{SS} + 0.2V$ or $\geq V_{DD} - 0.2V$) (V_{DD} = max, f = 0 MHz)	I_{SB2}	9	12	mA

Note: 1. All active current measurements are measured with one address transition per cycle and at minimum cycle time.

3. Timing Specifications

Table 3-1. Capacitance[1]

Parameter	Symbol	Typical	Max	Unit
Address input capacitance	C_{In}	–	6	pF
Control input capacitance	C_{In}	–	6	pF
Input/Output capacitance	$C_{I/O}$	–	8	pF

Note: 1. f = 1.0 MHz, dV = 3.0V, T_A = 25°C, periodically sampled rather than 100% tested.

Table 3-2. AC Measurement Conditions

Parameter	Value	Unit
Logic input timing measurement reference level	1.5V	V
Logic output timing measurement reference level	1.5V	V
Logic input pulse levels	0 or 3.0 V	V
Input rise/fall time	2	ns
Output load for low and high impedance parameters	See Figure 3-1	
Output load for all other timing parameters	See Figure 3-2	

Figure 3-1. Output Load Test Low and High

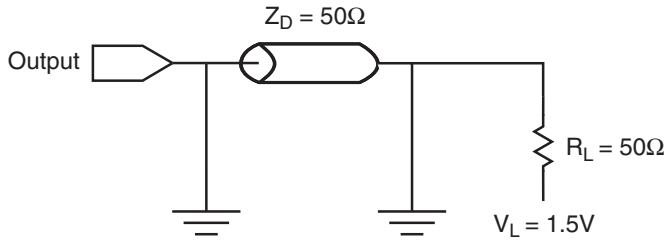


Figure 3-2. Output Load Test All Others

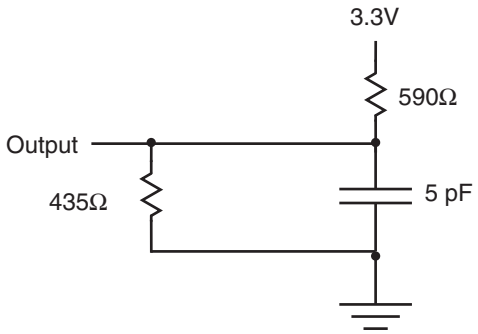
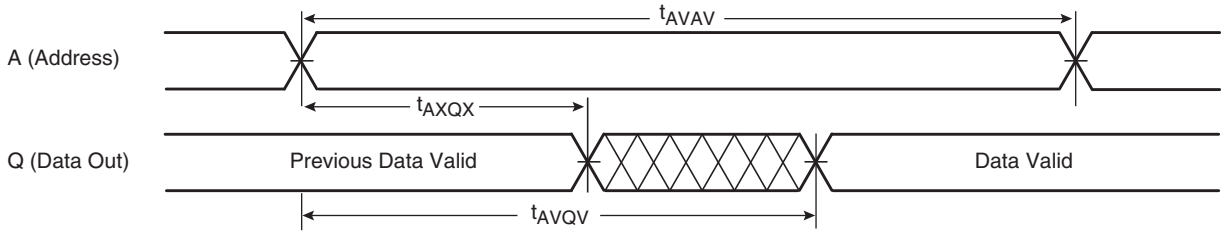


Table 3-3. Read Cycle Timing[1]

Parameter	Symbol	Min	Max	Unit
Read cycle time	t_{AVAV}	35	–	ns
Address access time	t_{AVQV}	–	35	ns
Enable access time[2]	t_{ELQV}	–	35	ns
Output enable access time	t_{GLQV}	–	15	ns
Byte enable access time	t_{BLQV}	–	15	ns
Output hold from address change	t_{AXQX}	3	–	ns
Enable low to output active[3]	t_{ELQX}	3	–	ns
Output enable low to output active[3]	t_{GLQX}	0	–	ns
Byte enable low to output active[3]	t_{BLQX}	0	–	ns
Enable high to output Hi-Z[3]	t_{EHQZ}	0	15	ns
Output enable high to output Hi-Z[3]	t_{GHQZ}	0	10	ns
Byte high to output Hi-Z[3]	t_{BHQZ}	0	10	ns

Notes: 1. $\overline{W}$ is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.
2. Addresses valid before or at the same time $\overline{E}$ goes low.
3. This parameter is sampled and not 100% tested. Transition is measured ±200 mV from the steady-state voltage.

Figure 3-3. Read Cycle 1



Note: Device is continuously selected ($\overline{E} \leq V_{IL}$, $\overline{G} \leq V_{IL}$)

Figure 3-4. Read Cycle 2

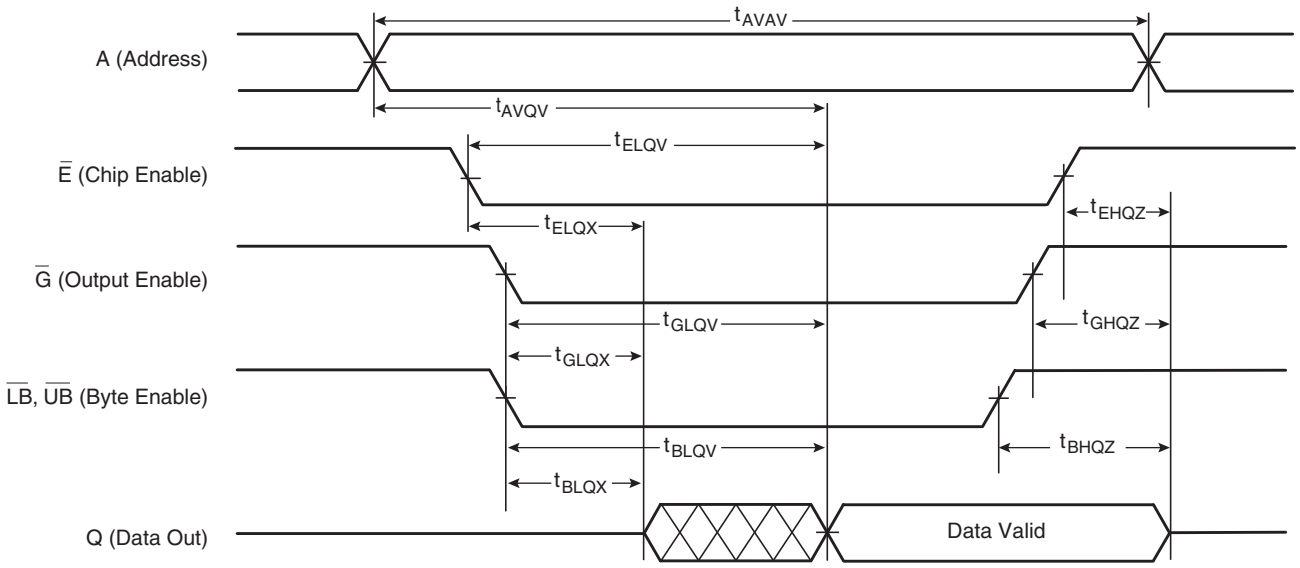


Table 3-4. Write Cycle Timing 1 ($\overline{W}$ Controlled)[1]

Parameter	Symbol	Min	Max	Unit
Write cycle time[2]	t_{AVAV}	35	–	ns
Address set-up time	t_{AVWL}	0	–	ns
Address valid to end of write (G high)	t_{AVWH}	18	–	ns
Address valid to end of write (G low)	t_{AVWH}	20	–	ns
Write pulse width (G high)	t_{WLWH}/t_{WLEH}	15	–	ns
Write pulse width (G low)	t_{WLWH} t_{WLEH}	15	–	ns
Data valid to end of write	t_{DVWH}	10	–	ns
Data hold time	t_{WHDX}	0	–	ns
Write low to data Hi-Z[3]	t_{WLQZ}	0	12	ns
Write high to output active[3]	t_{WHQX}	3	–	ns
Write recovery time	t_{WHAX}	12	–	ns

Notes:
1. All write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state. After $\overline{W}$, $\overline{E}$ or $\overline{UB}/\overline{LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between $\overline{E}$ being asserted low in one cycle to E being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. This parameter is sampled and not 100% tested. Transition is measured ±200 mV from the steady-state voltage. At any given voltage or temperate, t_{WLQZ}(max) < t_{WHQX}(min)

Figure 3-5. Write Cycle Timing 1 ($\overline{W}$ Controlled)[1]

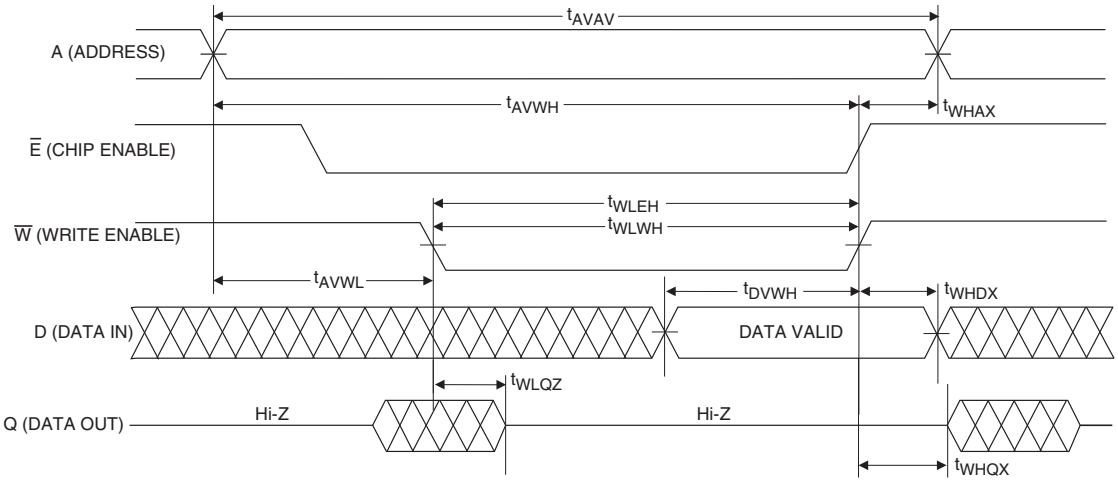


Table 3-5. Write Cycle Timing 2 ($\overline{E}$ Controlled)[1]

Parameter	Symbol	Min	Max	Unit
Write cycle time[2]	t_{AVAV}	35	–	ns
Address set-up time	t_{AVEL}	0	–	ns
Address valid to end of write ($\overline{G}$ high)	t_{AVEH}	18	–	ns
Address valid to end of write ($\overline{G}$ low)	t_{AVEH}	20	–	ns
Enable to end of write ($\overline{G}$ high)	t_{ELEH} t_{ELWH}	15	–	ns
Enable to end of write ($\overline{G}$ low)[3]	t_{ELEH} t_{ELWH}	15	–	ns
Data valid to end of write	t_{DVEH}	10	–	ns
Data hold time	t_{EHDX}	0	–	ns
Write recovery time	t_{EHAX}	12	–	ns

Notes:
1. All write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state. After $\overline{W}$, E or $\overline{UB}$/$\overline{LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between $\overline{E}$ being asserted low in one cycle to E being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. If $\overline{E}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high-impedance state. If $\overline{E}$ goes high at the same time or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

Figure 3-6. Write Cycle Timing 2 ($\overline{E}$ Controlled)

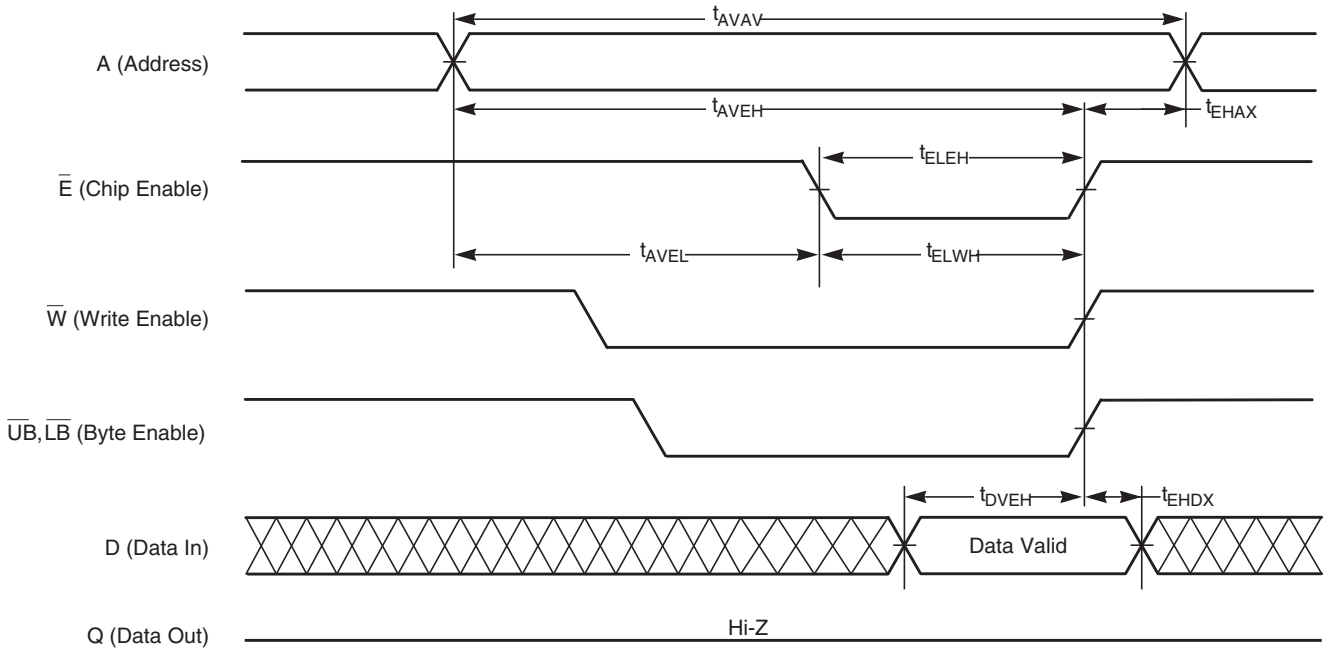
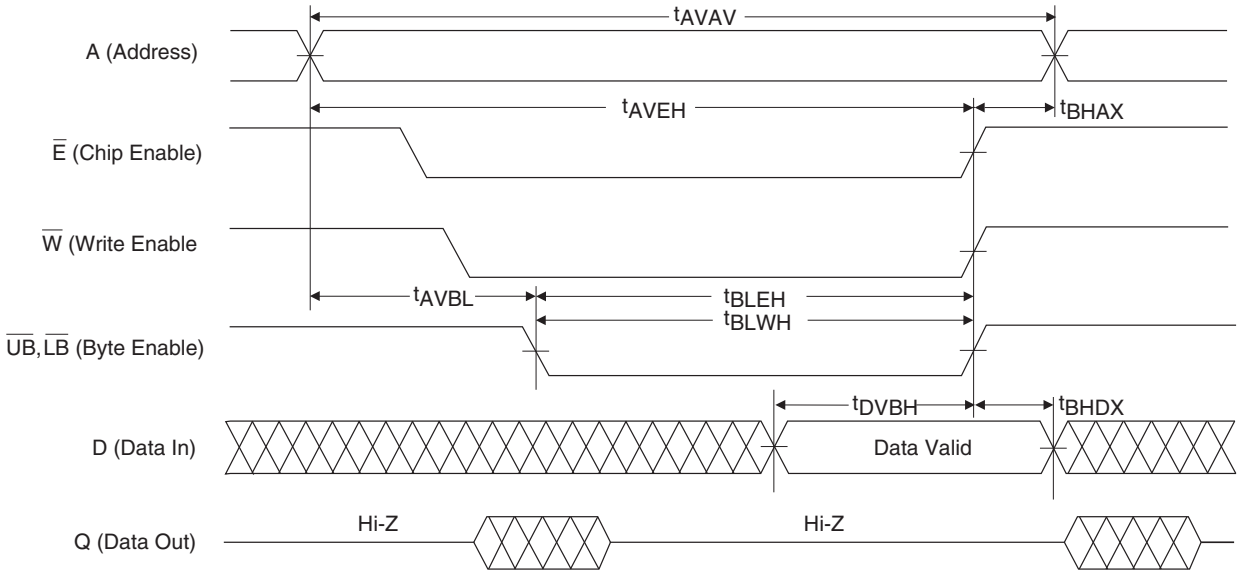


Table 3-6. Write Cycle Timing 3 ($\overline{LB}$/$\overline{UB}$ Controlled)[1]

Parameter	Symbol	Min	Max	Unit
Write cycle time[2]	t_{AVAV}	35	–	ns
Address set-up time	t_{AVBL}	0	–	ns
Address valid to end of write ($\overline{G}$ high)	t_{AVBH}	18	–	ns
Address valid to end of write ($\overline{G}$ low)	t_{AVBH}	20	–	ns
Write pulse width ($\overline{G}$ high)	t_{BLEH} t_{BLWH}	15	–	ns
Write pulse width ($\overline{G}$ low)	t_{BLEH} t_{BLWH}	15	–	ns
Data valid to end of write	t_{DVBH}	10	–	ns
Data hold time	t_{BHDX}	0	–	ns
Write recovery time	t_{BHAX}	12	–	ns

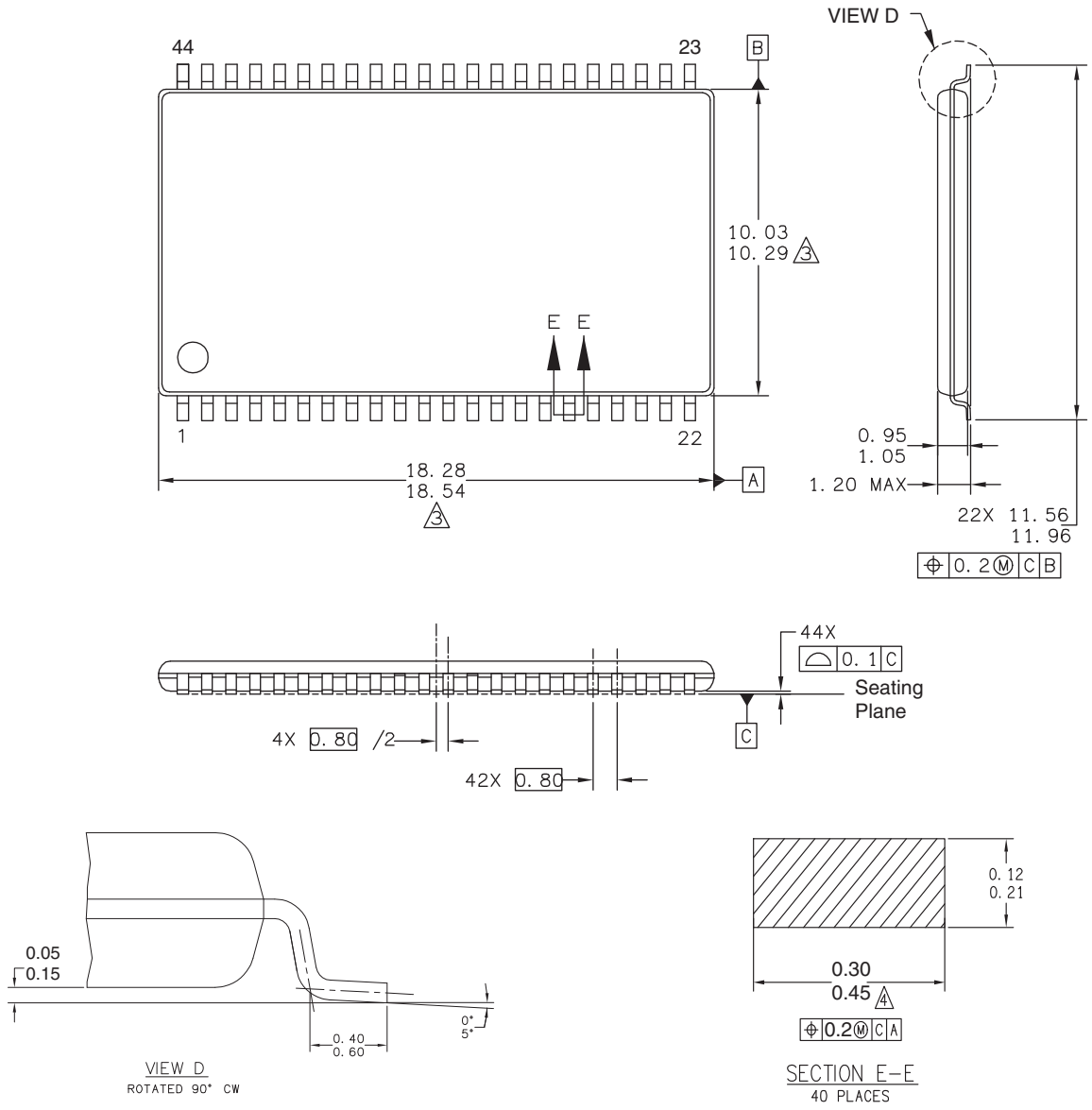
Notes:
1. All write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state. After $\overline{W}$, $_E$ or $\overline{LB}$/$\overline{UB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. If both byte control signals are asserted, the two signals must have no more than 2 ns skew between them. The minimum time between $\overline{E}$ being asserted low in one cycle to E being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.

Figure 3-7. Write Cycle Timing 3 ($\overline{LB}$/$\overline{UB}$ Controlled)



4. Mechanical Drawing

Figure 4-1. 44-TSOP2



Print Version Not To Scale

1. Dimensions and tolerances per ASME Y14.5M - 1994.
2. Dimensions in Millimeters.
3. Dimensions do not include mold protrusion.
4. Dimension does not include DAM bar protrusions.
   DAM Bar protrusion shall not cause the lead width to exceed 0.58.

5. Ordering Information

This product is available in Industrial and Military temperature versions.

Figure 5-1. Ordering Information

EV	2	A	16	A	x	N	Y	U	35
	Density Code	Memory Type	I/O Configuration	Revision	Operating Temperature Range	Package Type	RoHS compliance	Upscreening	Timing Set
e2v Prefix	2 = 4 Mb	A = async	16 = 16 bits	A =180 mm	V = -40 to 110˚C M = -55 to 125˚C	(N = TSOP II)	Y: RoHS(2) compliant	U	(35 = 35 ns)

Notes: 1. For availability of the different versions, contact your local e2v sales office.
2. Lead finishing: pure tin (Sn 99,99%)

6. Document Revision History

Table 6-1 provides a revision history for this hardware specification.

Table 6-1. Document Revision History

Rev. No	Date	Substantive Change(s)
0918E	02/2013	Corrected error in Table 1-1, “Pin Functions,” on page 2. Corrected Figure 3-1 on page 6.
0918D	06/2012	Updated picture page 1.
0918C	09/2010	Updated Table 2-2 on page 4.
0918B	06/2009	Add Section 2.2 ”Power-up and Power-down Sequencing” on page 5. Correct Ioh spec to 100 µA Correct AC test conditions.
0918A	12/2007	Table 1-2: Changed I_{DDA} to I_{DDR} or I_{DDW} Figure 5-1: Added RoHS compliance status in the part number.
0918AX	11/2007	Initial revision.

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